Remarks/Arguments

Claims 1, 3, 5, and 13-22 are pending in the present application before the present amendment. By the present amendment, claim 1 has been amended. No new matter has been added.

In the final office action, pages 2-3, mailed November 26, 2011, claims 1, 3, 5, and 21-23 stand rejected under 35 U.S.C. 112, first paragraph, as failing to comply with written description requirement.

The applicants respectfully **disagree**.

The examiner alleges that the present application lacks positive recitation to support the clause "…without use of a compensating resistor to generate the voltage attenuation quantity" and asks the applicants to "cite the portion of the specification explaining how the voltage attenuation quantity is generated, which necessarily excludes the use of a compensating resistor."

In the Background section of the present application (see page 6-7), the applicants have admitted as prior art a technique of having to physically compensate resistance value (which could include utilizing a compensating resistor) to compensate for the varying gate on/off voltage levels in the serially connected gate driver ICs 20 (see FIG. 2 Prior Art) due material/thickness/width/length variation in the signal line patterns that affects the voltage variations in the gate driver ICs 20. The applicants also disclosed that this prior art technique have many problems for which the present application provides an effective solution.

> "Still another [conventional] method is to **coincide a resistance value** of an inside signal line patterns existed in the gate driver ICs 20 with that of the signal line patterns of the panel so that non-uniformity of a screen caused at boundary faces among the gate driver ICs 20 is reduced. **However, this method has an economic problem in that design of the gate driver ICs 20 must be changed every time according to several variables, such as size and resolution of a liquid crystal panel, etc.**" (Specification page 6, line 19 to page 7, line 3)

The applicants respectfully note that the above admission of prior art refers to the physical alteration of resistance by utilizing, for example, a compensating resistor as in the case of the cited US 2003/0117456 (Moon). It has been also admitted in the Specification Background pages 3-4 with respect to FIG. 2 that the undesired voltage

variation occur due to the resistance created by the physical characteristics of the signal line patterns 22 connecting gate driver ICs 20.

To clearly set forth this in claim 1 without causing ambiguity, claim 1 has been amended as follows without adding any new matter:

> ~~**--without use of a compensating resistor**~~ to generate the voltage attenuation quantity **without physically compensating a resistance value variation inside a gate driver IC**--.

The applicants respectfully submit that this amendment will render moot the examiner's contention related to recital of "compensating resistor" in claim 1. No new matter is contained in the amendment to render a new search as there is no new ground for a new search with respect to --without physically compensating a resistance variation-- versus "without using a compensating resistor." On this ground, a reply of advisory action not entering the above amendment is believed to be improper; however, in case when the examiner disagrees, the applicants respectfully request for reasons as to how new grounds for additional search can be present.

Furthermore, an embodiment of the present invention described the specification page 21, line 17 to page 23, line 1 fully supports the invention of claim 1 that performs to compensate for variation of each voltage caused in each gate driver IC **without physically compensating a resistance value variation inside a gate driver IC**.

As clearly set forth in MPEP 2129I-II (stated below), such as above disclosure in the specification identifying work done by another as prior art must treated as prior art, and thus, this admission of prior art disclosure **necessarily excludes** the possibility of using a compensating resistor in the present disclosure and claimed invention.

> **2129 Admissions as Prior Art**
> **I. ADMISSIONS BY APPLICANT CONSTITUTE PRIOR ART**
> A statement by an applicant in the specification or made during prosecution identifying the work of another as "prior art" is an admission which can be relied upon for both anticipation and obviousness determinations, regardless of whether the admitted prior art would otherwise qualify as prior art under the statutory categories of 35 U.S.C. **102**.
> **II. DISCUSSION OF PRIOR ART IN SPECIFICATION**
> Where the specification identifies work done by another as "prior art," the subject matter so identified is treated as admitted prior art.

At least on the grounds above, the applicants respectfully submit that the rejection under 35 U.S.C. 112, first paragraph has been overcome. Withdrawal of the rejection is respectfully requested.

In the final office action pages 4-8, claims 1, 3, 5, 21, and 23 stand rejected under 35 U.S.C. 103(a) as being unpatentable over US 2003/0117456 (Moon) in view of US 5,764,212 (Nishtani) and US 6,232,944 (Kumagawa).

With respect to the rejection above, the applicants respectfully reassert the argument of the last filed amendment that Moon (individually or in combination with other cited references) fails to teach or suggested the present invention of claim 1 as amended.

The applicant thanks the examiner's response to the applicant's earlier argument that the cited Moon reference cannot and does not teach the claimed --sequence recognition unit--. The applicant does not agree, but, regardless, the applicant respectfully wishes to distinctly point out that Moon and the presently claimed invention are quite different from each other.

The applicant has already pointed out the following in the last filed amendment that the presently claimed invention solves the problems associated with the voltage drops in the signal line pattern 22 as shown in FIG. 2 (Prior Art). For example, referring to FIG. 7, there would be voltage drop of Vs = Ig x Rp across the gate driver IC 44 (where Ig is the current and Rp is the overall resistance). To solve this problem, the presently invention teaches specifically --a gate on-off voltage generation unit-- that can adjust the voltage by, for example, by **subtracting** a **voltage attenuation quantity** corresponding to the location data of the gate driver IC from the first gate-off voltage **without physically compensating a resistance value variation inside a gate driver IC to generate the voltage attenuation quantity**. The applicant emphasizes again that **no** need for a physical compensation such as a compensation resistor is required or used in a gate driver IC to adjust for the voltage drop across. Rather, the voltage value to be offset (e.g., the voltage attenuation quantity) is generated according to, inter alia, --the location data-- of the gate driver IC.

In the Background section of the specification page 6, line 19 to page 7, line 3, the presently invention specifically rejects using resistors inside signal line patterns in

gate driver ICs, because this will create design problems in that the design of the gate driver ICs must be changed every time according to several variables.

The applicant respectfully refers again to Moon [0055], in which Moon specifically teaches compensating resistance inside a gate drive IC using a physical device such as "**a compensating resistor … within each of the gate driver ICs 48A to 48D**." Moon clearly teaches using "compensating resistance values for each of the compensating resistors" in [0056 towards the end of the paragraph], and there are no other disclosure in Moon other than [0055] and [0056] that addresses the problems related to compensating for voltage difference.

Clearly, for the reasons above, Moon individually or in combination with Nishtani and Kumagawa do not teach claim 1 as amended. Withdrawal of rejection and an indication of allowable subject matter are respectfully requested

In the office action page 8, claims 13-20 are allowed. The applicants thank the examiner.

For the reasons set forth above, allowance of all pending claims 1, 3, 5, and 13-22 are respectfully requested in the next action.

The examiner is encouraged to contact the undersigned attorney by telephone to resolve any issues remaining.

Respectfully submitted,

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